REMARKS

In the Office Action, claims 1, 2, 6, 7, and 17 are rejected pursuant to 35 U.S.C. § 102 in view of U.S. Patent No. 6,045,626 ("Yano"); claims 3 and 5 are rejected under 35 U.S.C. § 102 in view of U.S. Patent No. 6,291,257 ("Kadota"); claims 8, 9, and 19 are rejected under 35 U.S.C. § 103 in view of Yano and further in view of U.S. Patent No. 6,806,503 ("Hosono"); claims 10, 11, 15, and 16 are rejected pursuant to 35 U.S.C. § 103 in view of Kadota and further in view of U.S. Patent No. 6,146,916 ("Nanishi"); claims 12, 13, 18, and 20 are rejected for alleged obviousness reasons in view of Kadota, Nanishi and further in view of Hosono; and claims 4, 14, and 21 are rejected for alleged obviousness reasons in view of Kadota, Nanishi, and Hosono.

As previously provided, claims 1-21 have been canceled without prejudice or disclaimer. Therefore, the rejections with respect to claims 1-21 should be rendered moot and thus withdrawn.

Further, Applicants have added new claims 22-30. Applicants believe that the newly added claims should be considered patentable over the cited art of record. For example, claim 22 recites a nitride semiconductor device with a nitride semiconductor layer including an InN crystal formed on a YSZ substrate with an atomic step regularly formed thereon, and further showing a half value width of a peak below 1.0° associated with an XRD spectrum. New claim 23 which depends from claim 22 further recites the nitride semiconductor layer showing the half value width of the peak below 0.5° associated with the XRD spectrum.

Independent new claim 24 recites a nitride semiconductor device that includes, in part, a GaN crystal layer formed on a ZnO substrate wherein the nitride semiconductor layer shows a half life width of a peak below 1.0° associated with an XRD spectrum. New claim 25 depends from claim 24 and further recites that the nitride semiconductor layer shows the half value width of the peak below 0.5° associated with the XRD spectrum.

New claim 26 recites a method for the preparation of a nitride semiconductor device having a nitride semiconductor layer formed of InN. The method includes, in part, polishing a plane (111) of a YSZ substrate up to an rms value of a surface roughness of 10 Å or less. New claim 27 depends from claim 26 and further defines that in the vapor deposition step, the InN is vapor-deposited by a PLD method. New claim 28 recites a method for preparing a nitride

semiconductor device having a nitride semiconductor layer formed of InGaN as further specified in claim 28. Claim 28 recites in part polishing a (000-1) plane or a (0001) plane of a ZnO substrate up to a rms value of a surface roughness of 10 Å or less. New claims 29 and 30 depend from claim 28. Claim 29 further recites that $In_xGa_{1-x}N$ ($0 \leq x \leq 0.4$) is vapor-deposited by a PLD method; and claim 30 further recites that $In_xGa_{1-x}N$ ($0 \leq x \leq 0.4$) is vapor-deposited at an ambient temperature.

Based on at least these differences as discussed above, Applicants believe that the cited references, even if combinable in any hypothetical combination, is distinguishable from new claims 22-30.

For the foregoing reasons, Applicants believe that the present application is in condition for allowance and earnestly solicit reconsideration of same.

The Commissioner is hereby authorized to charge deposit account 02-1818 for any fees which are due and owing.

Respectfully submitted,

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